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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: **FUJIWARA, Hideaki**

Serial No.: **09/899,267**

Filed: **July 6, 2001**

Group Art Unit: **2822**

Examiner: **ROSE, Kiesha L.**

P.T.O. Confirmation No.: **3927**

For. **SEMICONDUCTOR MEMORY AND SEMICONDUCTOR DEVICE**

AMENDMENT UNDER 37 CFR §1.111

Commissioner for Patents
Washington, D.C. 20231

November 18, 2002

Sir:

In response to the Office Action dated **August 20, 2002**, please amend the above-identified application as follows:

IN THE CLAIMS:

AMEND claims 2 and 5 to read as follows:

A1

2. (AMENDED) The semiconductor memory according to claim 1, wherein a negative voltage is applied to said first source/drain region for erasing.

A2

5. (AMENDED) The semiconductor memory according to claim 3, wherein said second impurity region is capacitively coupled with said floating gate electrode through a first insulator film.